WHAT IS CLAIMED IS:

1. A semiconductor data processing device for connecting a non-volatile storage device to a general-purpose bus of a host system, in which said data processing device enters an active state or standby state in response to a state of said general-purpose bus,

said data processing device comprising:

a clock circuit for stopping an internal clock signal in said standby state; and

a voltage generation circuit for applying a substrate bias voltage in a direction for reducing a threshold leak current in said standby state.

2. The semiconductor data processing device further comprising:

a rewritable non-volatile memory for storing a control program that connecting said non-volatile storage device to said general-purpose bus; and

a central processing unit for executing said control program,

wherein said central processing unit and said non-volatile memory receive said substrate bias voltage.

3. The semiconductor data processing device according to claim 2, further comprising a circuit for detecting the state

of said general-purpose bus to control state changes from said standby state to said active state,

wherein said substrate bias voltage is not applied to any of this circuit and said voltage generation circuit.

4. The semiconductor data processing device according to claim 3, further comprising a first interface controller that interfaces with said non-volatile storage device.

5. The semiconductor data processing device according to claim 4, further comprising a second interface controller that interfaces with said general-purpose bus.

6. The semiconductor data processing device according to claim 5,

wherein said first interface controller is a memory card interface controller and said second interface controller is a USB interface controller.

7. The semiconductor data processing device according to claim 5 or 6, further including a data transfer controller for controlling data transfer between said first interface controller and said second interface controller.

8. The semiconductor data processing device according to claim 7,

wherein said first and second interface controllers, as well as said data transfer controller input/output parallel data in units of 2n bits while said central processing unit inputs/outputs parallel data in units of n bits or below.

9. The semiconductor data processing device according to claim 8,

wherein said data transfer controller is connected to a 2n-bit first data bus while said central processing unit is connected to either the lower part or upper part of said first data bus.

10. The semiconductor data processing device according to claim 9,

wherein said first and second interface controllers are connected to a 2n-bit second data bus respectively,

wherein said processing device further includes a first data bus for connecting said first data bus to said second data bus, and

wherein said bus controller fixes the correspondence between each signal line of said second bus and the bit position of access data and varies the correspondence between each signal line of said first data bus and the bit position of access data according to each access data size.

11. A semiconductor data processing device, comprising:

a central processing unit; and

a rewritable non-volatile memory for storing a program to be executed by said central processing unit,

wherein an internal clock signal is stopped and a substrate bias voltage is applied in a direction for increasing a threshold voltage in the standby state, and said

substrate bias voltage is also applied to said central processing unit and said non-volatile memory.

12. The semiconductor data processing device according to claim 11, further comprising:

first and second interface controllers controlled by said central processing unit; and

a data transfer controllers capable of controlling data transfer between said first and second interface controllers.

13. The semiconductor data processing device according to claim 12,

wherein said first interface controller is a memory card interface controller.

14. The semiconductor data processing device according to claim 12,

wherein said second interface controller is a USB interface controller.

15. The semiconductor data processing device according to claim 12,

wherein said first and second interface controllers, as well as said data transfer controller input/output parallel data in units of 2n bits while said central processing unit inputs/outputs parallel data in units of n bits or below.

16. The semiconductor data processing device according to claim 15,

wherein said data transfer controller is connected to a 2n-bit first data bus while the central processing unit is connected to either the lower or upper part of said first data bus.

17. The semiconductor data processing device according to claim 16,

wherein said first and second interface controllers are connected to a 2n-bit second data bus respectively,

wherein said processing device includes a bus controller for connecting said first data bus to said second data bus, and

wherein said bus controller fixes the correspondence between each signal line of said second bus and the bit position of access data and varies the correspondence between each signal line of said first data bus and the bit position of access data according to the access data size.

18. A semiconductor data processing device, comprising:

a first peripheral circuit that inputs/outputs parallel data in units of 2n bits;

a second peripheral circuit that inputs/outputs parallel data in units of 2n bits;

a data transfer controller capable of controlling data transfer between said first and second peripheral circuits that input/output data in parallel in units of 2n bits;

a 2n-bit first data bus connected to said data transfer controller; and

a central processing unit that processes parallel data in units of n bits or below, connected to either the lower or upper part of said first data bus.

19. The semiconductor data processing device according to claim 18,

wherein said first and second peripheral circuits are connected to said 2n-bit second data bus respectively, and

wherein said processing device further includes a bus controller for connecting said first data bus to said second data bus.

20. The semiconductor data processing device according to claim 19,

wherein said bus controller fixes the correspondence between each signal line of said second bus and the bit position of access data and varies the correspondence between each signal line of said first data bus and the bit position of access data according to each access data size.

21. A data processing system comprising a bridge circuit for connecting a non-volatile storage device to a general-purpose bus,

wherein said bridge circuit includes a semiconductor data processing device for controlling data transfer between said general-purpose bus and said non-volatile storage device,

wherein said semiconductor data processing device includes a data transfer controller, a central processing unit, and a rewritable non-volatile memory for storing a control program, changes its state from active to standby in response to the state of said general-purpose bus, and stops an internal clock signal and applies a substrate bias voltage in a direction for reducing a sub-threshold leak in said standby state to change the state from said standby to said active in response to the second state that follows said first state.

22. The data processing system according to claim 21,

wherein said substrate bias voltage is applied to said central processing unit and said non-volatile memory in said standby state.

23. The data processing system according to claim 21 or 22,

wherein said non-volatile storage device is a non-volatile memory card, said general-purpose bus is a USB bus, said first state is an idle state, and said second state is a communication requesting state.

24. A semiconductor data processing device, comprising:

a central processing unit;

a non-volatile memory for storing a control program to be executed in said central processing unit, said memory capable of writing and erasing data therein/therefrom electrically;

a clock generation circuit; and

a first control circuit,

wherein said clock generation circuit stops generation of said clock when said data processing device enters said standby state while said first control circuit controls said central processing unit, said non-volatile memory, and said clock generation circuit so as to reduce a sub-threshold leak current in each MOS transistor constituting said central processing unit, said non-volatile memory, and said clock generation circuit.

25. The semiconductor data processing device according to claim 24,

wherein said first control circuit receives first and second supply potentials to be driven to operate regardless of whether said data processing device is in said standby state or not.

26. The semiconductor data processing device according to claim 25, further including a peripheral circuit,

wherein said peripheral circuit includes a first detection circuit for detecting the state of a bus to which it is be connected,

wherein said first control circuit controls the elements of said peripheral circuit except for said first detection circuit in response to said standby state, and

wherein said first detection circuit receives first and second supply potentials to be driven to operate regardless of

whether or not said data processing device is in said standby state.

27. The semiconductor data processing device according to claim 26,

wherein said processing device further includes a second control circuit,

wherein said second control circuit includes a second detection circuit for detecting the output of said first detection circuit,

wherein said first control circuit controls circuit elements of said second control circuit other than said second detection circuit in response to said standby state, and

wherein said second detection circuit receives said first and second supply potentials to be driven to operate regardless of whether or not said data processing device is in said standby state.

28. A data processing system comprising a bridge circuit for connecting a non-volatile storage device to a general-purpose bus,

wherein said bridge circuit includes a semiconductor data processing device for controlling data transfer between said general-purpose bus and said non-volatile storage device,

wherein said semiconductor data processing device includes a data transfer controller, a central processing unit, a rewritable non-volatile memory for storing a control program

to be executed in said central processing unit, a clock generation circuit, and a first control circuit,

wherein said semiconductor data processing device changes the state from said standby to said active in response to the first state of said general-purpose bus,

wherein said clock generation circuit stops generation of said clock signal in said standby state,

wherein said control circuit controls said central processing unit, said non-volatile memory, and said clock generation circuit so as to reduce the sub-threshold leak current of each MOS transistor constituting said central processing unit, said non-volatile memory, and said clock generation circuit, and

wherein said semiconductor data processing device changes the state from said standby to said active in response to the second state of said general-purpose bus, said second state following said first state.

29. The data processing system according to claim 28,

wherein said first control circuit of said semiconductor data processing device receives said first and second supply potentials and is driven to operate regardless of whether or not said data processing device is in said standby state.

30. The data processing system according to claim 29,

wherein said semiconductor data processing device further includes a peripheral circuit,

wherein said peripheral circuit includes a first detection circuit for detecting the state of said general-purpose bus,

wherein said first control circuit controls elements of said peripheral circuit except for said first detection circuit in response to said standby state, and

wherein said first detection circuit receives said first and second supply potentials and is driven to operate regardless of said standby state.

31. The data processing system according to claim 26,

wherein said semiconductor data processing device further includes a second control circuit,

wherein said second control circuit includes a second detection circuit for detecting the state of said first detection circuit,

wherein said first control circuit controls elements of said second control circuit except for said second detection circuit in response to said standby state, and

wherein said second detection circuit receives said first and second supply potentials and is driven to operate regardless of said standby state.